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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,463	03/30/2000	Charles W. Selvidge	M-8288 US	8093

22907 7590 02/23/2004

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/23/2004 10

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/539,463	Applicant(s) SELVIDGE ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3-3-2000.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 March 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4, 6 & 9.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been presented for Examination. Claims 1-16 have been Examined and rejected.

Drawings

2. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal Drawings will be required when the application is allowed. The drawings filed on 3/30/2003 are acceptable subject to correction of the formalities listed in the attached "Notice of Draft person's Patent Drawing Review," PTO-948.

2.1 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: *"emulation system 100"* as disclosed in lines 1-2 on page 5 of the specification does not appear in Figure 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-7 and 11-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample et al. U.S. Patent 5,690,191** in view of **Barr et al. 5,297,181.**

3.1 As regards independent **Claims 1 and 2** the *Sample et al.* reference discloses a logic emulation system **(Figure 1, Col. 6 Lines 39-57 & Figure 12),** providing a transmit clock signal of a predetermined clock frequency **(Figure 10 Item 144, Col. 19 Lines 15-29 and Figure 19 Item 200),** a method for transmitting a data packet between substantially asynchronous components **(Figure 10, Col. 13 Lines 43-62, Col. 14 Lines 6-10),** transmitting serially over a connection between asynchronous systems **(Col. 10 Lines 39-47, Col. 10 Lines 66-67, Col. 11 Lines 1-21)** and a framing sequence **(Col. 24 Lines 67, Col. 25 Lines 1-19).**

However the *Sample et al.* reference does not expressly disclose a framing sequence, subsequent to transmitting the framing sequence transmitting a data packet serially, and each bit of the framing sequence is transmitted over two transmit clock periods.

The *Sample et al.* reference discloses that, the use of serial data encoding techniques can reduce power consumption and increase the speed *(performance)* of the emulation system **(Col. 11 Lines 22-36).** An artisan of an ordinary level of skill would have looked in the high speed interface protocol art to find a method to send data over a asynchronous serial link and preserve

the clock information in order to lower the power consumption of the emulator and reduce the power consumption. In the digital communications art the *Barr et al.* reference discloses a framing sequence **(Figure 1 & Col. 1 Lines 30-37 & Col. 3 Lines 62-68),** subsequent to transmitting the framing sequence transmitting a data packet serially **(Col. 4 Lines 18-31),** and each bit of the framing sequence is transmitted over two transmit clock periods **(Figure 2(B) & Col. 2 Lines 40-47).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the emulation technology of the *Sample et al.* reference with the asynchronous digital communications technology of the *Barr et al.* reference because it is desirable to be able to synchronize over a wide range of sampling rates **(Barr et al. Col. 3 Lines 29-34).**

3.2 As regards independent **Claims 5 & 11** *see paragraph 3.1 above.* Further, as regards the limitation of having a plurality of programmable logic devices the *Sample et al.* reference discloses **(Col. 1 Lines 10-23),** and a controller coupled to a host computer **(Figure 14 Item 540).**

3.3 As regards dependent **Claim 3** the *Sample et al.* reference discloses different circuit boards in a chassis **(Figure 13).**

3.4 As regards dependent **Claims 4** the *Sample et al.* reference discloses a controller housed in a host computer **(Figure 19 Item 500).**

3.5 As regards dependent **Claims 6, 7, 12 & 13** the *Sample et al.* reference discloses a master clock signal being generated on a separate controller board **(Figure 19).**

4. **Claims 8-10 and 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample et al. U.S. Patent 5,690,191** in view of **Barr et al. 5,297,181** and in further view of **Marantz et al. U.S. Patent 6,061,511.**

4.1 As regards independent **Claims 5 and 11** see paragraphs **3.1** and **3.2** above.

4.2 As regards dependent **Claims 8-10** and **14-16** the *Sample et al.* reference does not expressly disclose *"virtual clocks"*.

The *Marantz et al.* reference discloses *Virtual Clocks* **(Col. 1 Lines 52-65 & Col. 2 Lines 66-67, Col. 3 Lines 1-9).**

It would have been obvious, to one of ordinary skill in the art, at the time the inventions was made, to have combined the emulation technology of the *Sample et al.* reference with the *Virtual Clock"* technology of the *Marantz et al.* reference because the *Virtual Clock* technology many conditions in the logic emulation can be faithfully produced that would otherwise not be properly emulated, **(Marantz et al. Col. 3 Lines 2-9).**

Conclusion

5. **Claims 1-16** have been rejected. This action is **NON-FINAL.**

5.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

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